CLAIMS

What is claimed is:

Sub B1

1. A display device comprising:

an array of display drivers, said display drivers including a first plurality of display drivers, wherein said display drivers control the display of a plurality of pixels in a display area and wherein said display drivers are located within said display area which is viewable;

said first plurality of display drivers comprising a first serial shift register having a first plurality of memory elements each corresponding to and coupled to one display driver of said first plurality of display drivers.

2. A display device as in claim 1 wherein display data for pixels in a first row of pixels are stored in said first plurality of memory elements and wherein said plurality of pixels are a two-dimensional array of pixels.

3. A display device as in claim 2 wherein a second plurality of display drivers comprise a second serial shift register having a second plurality of memory elements each corresponding to and coupled to one display driver of said second plurality of display drivers.

4. A display device as in claim 2 wherein said display drivers drive pixel electrodes which control a display medium which comprises one of (a) a liquid crystal

material; (b) an electrophoretic display material; (c) an organic light emitting diode (LED) material; or (d) a semiconductor LED material.

5. A display device as in claim 3 wherein display data for pixels in a second row of pixels are stored in said second plurality of memory elements.

6. A display device as in claim 1 wherein each display driver is formed in a first substrate and then removed from the first substrate and then separately, for each display driver, deposited onto a second substrate.

7. A display device as in claim 6 wherein each display driver is deposited onto said second substrate through a fluidic self-assembly process.

8. A display device as in claim 5 wherein said display data flows through said array along only one axis which is parallel with said first and said second rows.

9. A display device as in claim 8 wherein said display data is shifted through said array by a clock signal.

10. A display device as in claim 9 wherein said clock signal is distributed through said array along only said one axis.

11. An integrated circuit (IC) device comprising:

a substrate which includes an integrated circuit;

a plurality of functionally symmetric interface pads coupling said integrated circuit to a receptor site of an electronic device, said plurality of interface pads being arranged in said substrate such that said electronic device operates with said substrate mounted to the receptor site in any one of a plurality of orientations relative to said receptor site, and

wherein said integrated circuit comprises:

an instruction decoder coupled to at least one of said plurality of interface pads, said instruction decoder decoding an instruction received through said at least one of said plurality of interface pads and causing an operation of said integrated circuit.

12. An IC device as in claim 11 wherein said integrated circuit further comprises:

an instruction register coupled to said instruction decoder for storing said instruction;

a control bus coupled to said instruction register.

13. An IC device as in claim 11 wherein said instruction decoder further comprises:

a timing discriminator coupled to said at least one of said plurality of interface pads said timing discriminator discriminating between clocking signals and instruction data which represent said instruction.

14. An IC device as in claim 11 wherein said instruction decoder is capable of decoding a plurality of instructions.

15. An IC device as in claim 14 wherein said IC device is a display driver and wherein said plurality of instructions cause said display driver to control at least one pixel of a display.

16. An IC device as in claim 11 wherein said integrated circuit further comprises:

a shift register coupled to at least one of said plurality of interface pads, said shift register shifting data stored in said shift register under control of said instruction.

17. An IC device as in claim 11 wherein said integrated circuit further comprises:

a position detector coupled to at least one of said plurality of interface pads, said position detector detecting a position of said integrated circuit relative to said receptor site.

18. An IC device as in claim 17 wherein said position detector provides a signal which is determined by said position.

19. An IC device as in claim 11 wherein said at least one of said plurality of interface pads provides both said instruction to said instruction decoder and clock signals for controlling clocked operations of said integrated circuit.

20. An integrated circuit (IC) comprising:

a semiconductor substrate having a plurality of pads for electrical interconnect to other circuitry;

a position detector coupled to at least one of said pads of said plurality of pads, said position detector detecting a position of said IC relative to a receptor substrate and providing a signal, internally within said semiconductor substrate, which is determined by said position.

21. An IC as in claim 20 wherein said position comprises at least one of a translational location on said receptor substrate or a rotational orientation of said IC relative to said receptor substrate.

22. An IC as in claim 20 wherein said plurality of pads comprises a first pad which is configurable depending upon said signal.

23. An IC as in claim 22 wherein said first pad is configurable as one of (a) an input pad, or (b) an output pad, or (c) a no-operation pad.

24. An IC as in claim 20 wherein at least one function of said IC is determined by said signal.

25. An IC as in claim 20 wherein said IC is capable of performing at least one of a plurality of functions and wherein said signal causes said IC to perform a selected subset of said plurality of functions.

26. An IC as in claim 20 wherein said position is specified by a conductive layer on said receptor substrate which makes electrical contact with said position detector through said at least one of said pads.

27. An IC as in claim 25 wherein said selected subset is determined by a conductive layer on said receptor substrate which makes electrical contact with said position detector through said at least one of said pads.

28. An integrated circuit (IC) comprising:

a semiconductor substrate having a plurality of pads for electrical interconnection to other circuitry;

a position detector coupled to at least a first pad of said plurality of pads, said position detector detecting a position of said IC relative to a receptor substrate, wherein said first pad is configurable as at least one of the following: an input pad or output pad or a no-operation pad as determined by said position.

29. An IC as in claim 28 wherein said position comprises at least one of a transitional location on said receptor substrate or a rotational orientation of said IC relative to said receptor substrate.

30. An IC as in claim 28 wherein said position detector provides a signal which causes said first pad to be configured and wherein said first pad is configurable as one of at least two of the following: an input pad or an output pad or a no-operation pad as determined by said position.

31. An IC as in claim 28 wherein said position is specified by a conductive layer on said receptor substrate which makes electrical contact with said position detector.

32. An assembly comprising:

a receptor substrate having a conductive layer disposed over at least a portion of said receptor substrate;

an integrated circuit (IC) having a plurality of pads for electrical interconnect to other circuitry, said IC having a position detector coupled to at least one of said pads which is coupled to said conductive layer, said position detector detecting a position of said IC relative to said receptor substrate and providing a signal which is determined by said position.

33. An assembly as in claim 32 wherein said IC is fabricated on a first substrate and separated from said first substrate and is mounted on said receptor substrate through a fluidic self-assembly process.

34. An assembly as in claim 32 wherein said position comprises at least one of a translational location on said receptor substrate or a rotational orientation of said IC relative to said receptor substrate.

35. An assembly as in claim 32 wherein said plurality of pads comprises a first pad which is configurable depending upon said signal.

36. An IC as in claim 35 wherein said first pad is configurable as one of (a) an input pad, or (b) an output pad, or (c) a no-operation pad.

37. An IC as in claim 32 wherein at least one function of said IC is determined by said signal.

38. An IC as in claim 32 wherein said IC is capable of performing at least one of a plurality of functions and wherein said signal causes said IC to perform a selected subset of said plurality of functions.

39. An IC as in claim 38 wherein said selected subset is determined by said conductive layer on said receptor substrate which makes electrical contact with said position detector through said at least one of said pads.

40. An IC as in claim 20 wherein said IC is functionally symmetric over a plurality of rotational orientations relative to said receptor substrate.

41. An assembly as in claim 32 wherein said IC is capable of performing a first function at a first translational location on said receptor substrate and is capable of performing a second function at a second translational location on said receptor substrate.

42. An integrated circuit device comprising:

a substrate which includes an integrated circuit (IC);

a plurality of functionally symmetric interface pads coupling said IC to a receptor site of an electronic device, said plurality of interface pads being arranged in said substrate such that said electronic device operates with said substrate mounted to the receptor site in any one of a plurality of orientations relative to said receptor site, wherein said plurality of interface pads comprises:

a reference voltage pad for receiving a reference voltage signal;

a power supply pad for receiving a power supply signal;

at least four output pads;

a first configurable pad which is configurable as one of at least two of the following: an input pad or an output pad or a no-operation pad;

a second configurable pad which is configurable as one of at least two of the following: an input pad or an output pad or a no-operation pad.

43. An IC device as in claim 42 wherein said reference voltage signal is ground and wherein said plurality of interface pads further comprise:

a clock pad for receiving a clock signal for controlling clocked operations of said IC;

a third configurable pad which is configurable as one of at least two of the following: an input pad, or an output pad or a no-operation pad;

a fourth configurable pad which is configurable as one of at least two of the following: an input pad, or an output pad or a no-operation pad;

four position indicator pads.

44. An IC device as in claim 43 wherein said plurality of interface pads comprise up to 25 pads arranged in an array up to 5×5 and wherein there are four reference voltage pads and four power supply pads and eight output pads.

45. An assembly comprising:

a receptor substrate having a conductive layer disposed over at least a portion of said receptor substrate;

an integrated circuit (IC) attached to said receptor substrate and having a plurality of interface pads, including at least one interface pad which is coupled to said conductive layer to receive a signal from said conductive layer, said IC also comprising:

a first logic circuit coupled to a first set said interface pads and providing a first function;

a second logic circuit coupled to a second set of said interface pads and providing a second function which is different than said first function;

a selector logic circuit coupled to said first logic circuit and coupled to said second logic circuit and coupled to receive said signal which causes said selector logic to select between said first function and said second function such that said IC performs only one of said first and said second functions.

46. An assembly as in claim 45 wherein said IC is attached to said receptor substrate through a fluidic self-assembly process, and wherein said first set and said second set of interface pads overlap at least partially.

47. An assembly as in claim 45 wherein said signal is determined by a position of said IC on said receptor substrate.

48. An assembly as in claim 47 wherein said position determines whether said IC provides said first function or said second function at said position.

49. An assembly as in claim 45 wherein said signal is a programming instruction which selects between said first and said second functions.

50. An assembly as in claim 45 wherein said first function is a sensing function and said second function is a presentation function.

51. An assembly as in claim 50 wherein said sensing function senses a touch of a user and said presentation function displays data to said user.

52. An assembly comprising:

a receptor substrate having an opening and a substantially planar region surrounding said opening and having a plurality of conductive layers attached over said substantially planar region;

an integrated circuit (IC) attached to said opening in said receptor substrate, said IC having electrical interface pads on a substantially planar surface which is substantially co-planar with said substantially planar region, said IC further comprising:

a first logic circuit coupled to a first set of said electrical interface pads and providing a first function;

a second logic circuit coupled to a second set of said electrical interface pads and providing a second function which is different than said first function.

53. An assembly as in claim 52 wherein said IC is attached to said receptor substrate through a fluidic self assembly process, and wherein said first set and said second set of electrical interface pads overlap at least partially.

54. An assembly as in claim 52 wherein said first function is a sensing function and said second function is a presentation function.

55. An assembly as in claim 52 wherein said IC is capable of performing both said first function and said second function substantially concurrently.

56. An integrated circuit (IC) comprising:

an instruction data logic coupled to an electrical interface pad, said instruction data logic receiving instruction commands to cause said IC to perform a particular function depending on a received instruction command;

a clocked logic circuit coupled to said electrical interface pad, said clocked logic circuit receiving a clock signal through said electrical interface pad which also provides said instruction commands to said IC.

57. An IC as in claim 56 further comprising:

a power supply circuit coupled to said electrical interface pad, said power supply circuit deriving power from said clock signal to generate a voltage rail signal for use within said IC.

58. An IC as in claim 56 wherein said clock signals control clocked operations of said clocked logic circuit.

59. An IC as in claim 58 wherein said instruction data logic comprises an instruction register for storing said received instruction command and wherein said clock signal is used to shift data within said IC.

60. A circuit comprising:

an input which receives a signal having first edges and second edges;

a pulse generation circuit which generates a pulse nested in time between consecutive first and second edges;

a power derivation circuit coupled to said input and coupled to said pulse generation circuit, said power derivation circuit generating a voltage value which is used by logic within said circuit.

61. A circuit as in claim 60 wherein said voltage value is a voltage rail supplying power to said logic.

62. A circuit as in claim 60 wherein each of said first edges is a rising edge and each of said second edges is a falling edge.

63. A circuit as in claim 60 wherein said input is coupled to an interface pad on an exterior surface of said circuit.

64. A circuit as in claim 60 wherein said signal is a clock signal which controls a clocked logic operation within said circuit.

65. A circuit as in claim 60 wherein said pulse causes said power derivation circuit to sample said signal to obtain a sampled signal and said sampled signal is stored in at least one storage capacitor.

66. A circuit as in claim 60 wherein said circuit is disposed within an integrated circuit.

67. A circuit as in claim 60 wherein said power derivation circuit is electrically de-coupled from said input when there is no pulse from said pulse generation circuit.

68. A display device comprising:

a two-dimensional (2-D) array of pixels;

an array of display drivers which are coupled to and which control said 2-D array of pixels, each of said display drivers receiving a clock signal

and a data signal, wherein said clock signal and said data signal are bussed only substantially parallel to one axis of said display.

69. A display device as in claim 68 wherein data in said data signal is shifted through said display under control of said clock signal.

70. A display device as in claim 68 wherein said display device comprises an active matrix backplane which includes said array of display drivers and wherein circuitry in said active matrix backplane including said array of display drivers, are interconnected with only a single electrically conductive interconnection layer which is attached to and disposed over said active matrix backplane.

71. A circuit for shifting a voltage level of a signal, said circuit comprising:
a first input to receive a clocked signal having a pulse during each clock cycle;
a second input to receive a first voltage signal;
a current mirror circuit coupled to said first input and coupled to said second input, said current mirror controlling a state of a node;
an output driver coupled to said node, said output driver shifting said first voltage signal to a second voltage signal when said node is at a first state.

72. A circuit as in claim 71 wherein said current mirror circuit comprises:
a first current path;

a second current path;

a first control electrode coupled to said first current path;

a second control electrode coupled to said second current path and coupled to said first control electrode.

73. A circuit as in claim 72 wherein said first control electrode is a first gate electrode of a first transistor device which is in said first current path and wherein said second control electrode is a second gate electrode of a second transistor device which is in said second current path and wherein said node is in said second current path and wherein said first transistor device and said second transistor device have respectively first and second size parameters which are substantially matched.

74. A circuit as in claim 73 wherein said pulse causes a current to flow in said second current path to set said node at said first state and wherein after said pulse, said node retains said first state with substantially no current flowing in said second current path.

75. A method for operating a circuit for shifting a voltage level of a signal, said method comprising:

receiving a first voltage signal;

receiving a clocked signal having a pulse during each clock cycle;

passing current through a first current path and a second current path which together form a current mirror, said current being passed when said

pulse is present, said second current path comprises a node which is set to a first state when current is passed through said second current path;

driving an output to a second voltage signal from said first state of said node.

76. A method for operating a circuit for shifting a voltage level of a signal, said method comprising:

receiving a first voltage signal;

receiving a clocked signal having repetitive clock cycles, each clock cycle having a corresponding pulse;

passing a current through a node during a first pulse of a first clock cycle to set said node at a first state, said node floating at substantially said first state during said first clock cycle after said first pulse;

driving an output to a second voltage signal from said first state of said node.

77. A method as in claim 76 wherein said driving occurs while said node is floating.

78. A method as in claim 77 wherein said floating occurs by disconnecting said node from power and ground reference voltage rails.

79. A circuit for shifting a voltage level of a signal, said circuit comprising:

a first input to receive a clocked signal having a pulse during each clock cycle;

a second input to receive a first voltage signal;

a driving node coupled to said first input and coupled to said second input, said driving node floating when said pulse is not present in a corresponding clock cycle;

an output driver coupled to said driving node, said output driver shifting said first voltage signal to a second voltage signal when said node is at a first state.

80. A circuit as in claim 79 wherein said output driver comprises an output transistor and said driving node is coupled to a control electrode of said output transistor.

81. A circuit as in claim 80 further comprising a current mirror circuit having a first current path coupled to a second current path and wherein said driving node is in said second current path.

82. A display device comprising:

a two-dimensional (2-D) array of pixels;

an array of display drivers which are coupled to and which control said 2-D array of pixels, each of said display drivers receiving a data signal, wherein said data signal is bussed only substantially parallel to one axis of said display and wherein said display device comprises an active matrix backplane which includes said array of display drivers

and wherein circuitry in said active matrix backplane including said array of display drivers, are interconnected with only a single interconnection layer which is attached to and disposed over said active matrix backplane.

83. A display device as in claim 82 wherein said pixels of said 2-D array of pixels is not arranged in rows and columns.